MJE13003

SWITCHMODE™ Series NPN Silicon Power Transistor

These devices are designed for high−voltage, high−speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V SWITCHMODE applications such as Switching Regulators, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

Features

- Reverse Biased SOA with Inductive Loads @ T_C = 100°C
- Inductive Switching Matrix 0.5 to 1.5 A, 25 and 100°C
  t_c @ 1 A, 100°C is 290 ns (Typ)
- 700 V Blocking Capability
- SOA and Switching Applications Information
- Pb−Free Package is Available*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	$V_{CEO(sus)}$	400	Vdc
Collector−Emitter Voltage	V_{CEV}	700	Vdc
Emitter Base Voltage	V_{EBO}	9	Vdc
Collector Current − Continuous − Peak (Note 1)	I_C I_{CM}	1.5 3	Adc
Base Current − Continuous − Peak (Note 1)	I_B I_{BM}	0.75 1.5	Adc
Emitter Current − Continuous − Peak (Note 1)	I_E I_{EM}	2.25 4.5	Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.4 11.2	W mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 320	W mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	3.12	°C/W
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	89	°C/W
Maximum Load Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

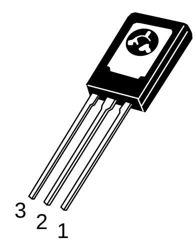
1. Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor®

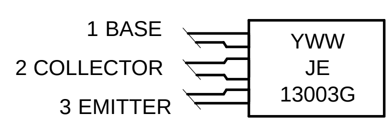
http://onsemi.com

1.5 AMPERES
NPN SILICON POWER TRANSISTORS
300 AND 400 VOLTS
40 WATTS



TO−225
CASE 77
STYLE 3

MARKING DIAGRAM



Y	=	Year
WW	=	Work Week
JE13003	=	Device Code
G	=	Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping
MJE13003	TO−225	500 Units/Box
MJE13003G	TO−225 (Pb−Free)	500 Units/Box

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (Note 2)					
Collector−Emitter Sustaining Voltage (I_C = 10 mA, I_B = 0)	$V_{CEO(sus)}$	400	−	−	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)	I_{CEV}	 − −	 − −	 1 5	mAdc
Emitter Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)	I_{EBO}	−	−	1	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with bass forward biased	$I_{S/b}$	See Figure 11			−
Clamped Inductive SOA with base reverse biased	RBSOA	See Figure 12			−
ON CHARACTERISTICS (Note 2)					
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 2 Vdc) (I_C = 1 Adc, V_{CE} = 2 Vdc)	h_{FE}	 8 5	 − −	 40 25	−
Collector−Emitter Saturation Voltage (I_C = 0.5 Adc, I_B = 0.1 Adc) (I_C = 1 Adc, I_B = 0.25 Adc) (I_C = 1.5 Adc, I_B = 0.5 Adc) (I_C = 1 Adc, I_B = 0.25 Adc, T_C = 100°C)	$V_{CE(sat)}$	 − − − −	 − − − −	 0.5 1 3 1	Vdc
Base−Emitter Saturation Voltage (I_C = 0.5 Adc, I_B = 0.1 Adc) (I_C = 1 Adc, I_B = 0.25 Adc) (I_C = 1 Adc, I_B = 0.25 Adc, T_C = 100°C)	$V_{BE(sat)}$	 − − −	 − − −	 1 1.2 1.1	Vdc
DYNAMIC CHARACTERISTICS					
Current−Gain − Bandwidth Product (I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 1 MHz)	f_T	4	10	−	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	−	21	−	pF

SWITCHING CHARACTERISTICS

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 125 Vdc, I_C = 1 A, I_{B1} = I_{B2} = 0.2 A, t_p = 25 μs, Duty Cycle ≤ 1%)	t_d	−	0.05	0.1	μs
Rise Time		t_r	−	0.5	1	μs
Storage Time		t_s	−	2	4	μs
Fall Time		t_f	−	0.4	0.7	μs
Inductive Load, Clamped (Table 1, Figure 13)						
Storage Time	(I_C = 1 A, V_{clamp} = 300 Vdc, I_{B1} = 0.2 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_{sv}	−	1.7	4	μs
Crossover Time		t_c	−	0.29	0.75	μs
Fall Time		t_{fi}	−	0.15	−	μs

2. Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

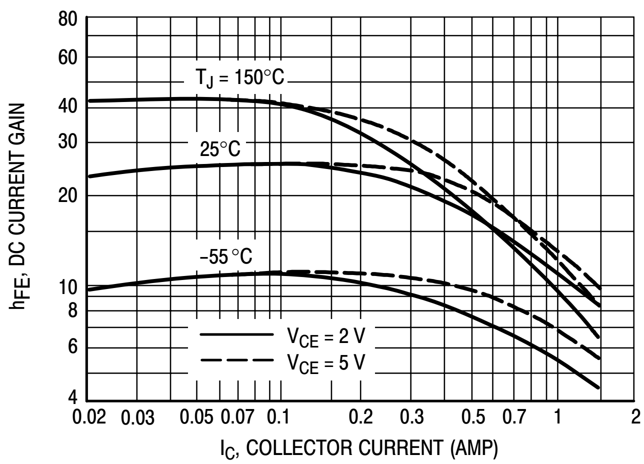


Figure 1. DC Current Gain

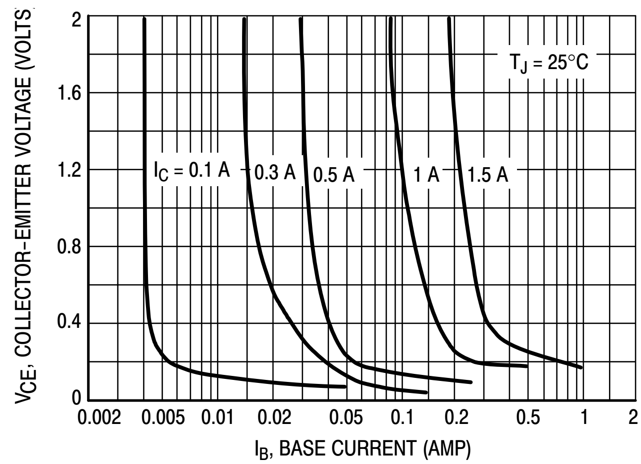


Figure 2. Collector Saturation Region

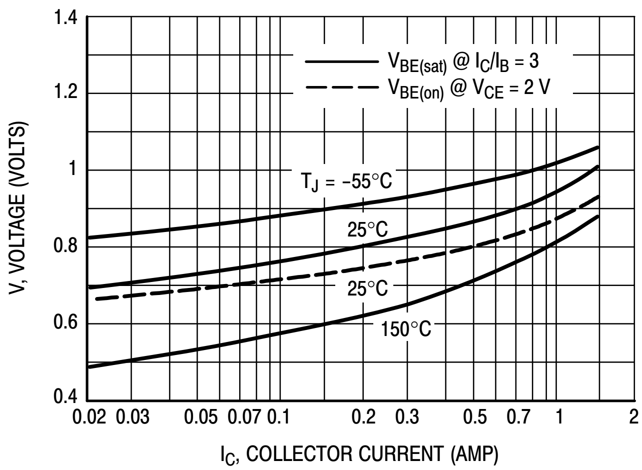


Figure 3. Base−Emitter Voltage

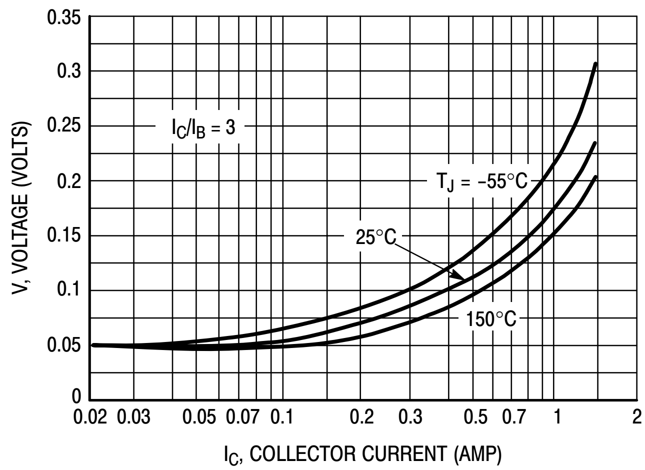


Figure 4. Collector−Emitter Saturation Region

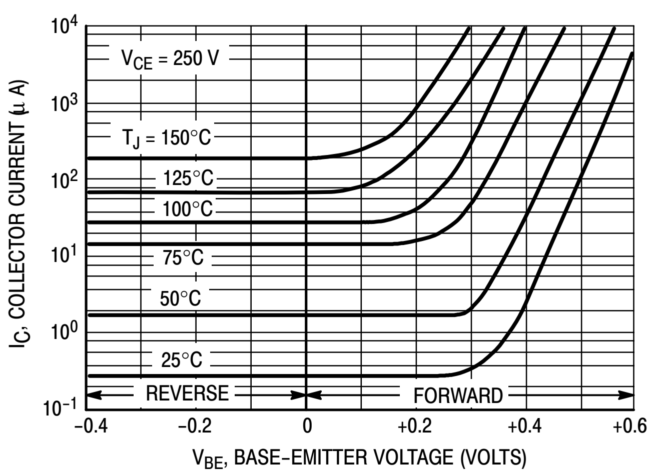


Figure 5. Collector Cutoff Region

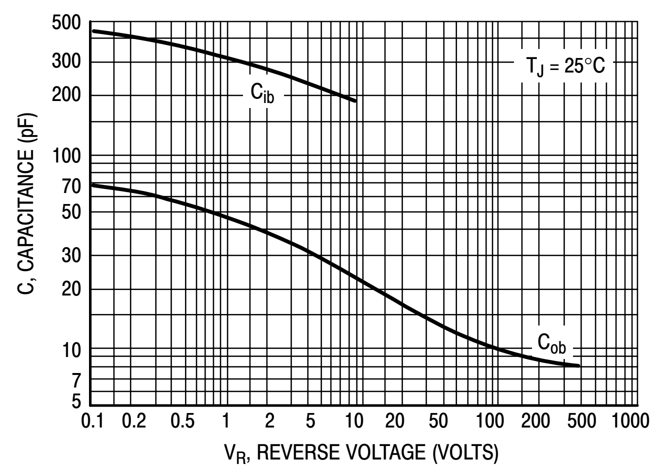
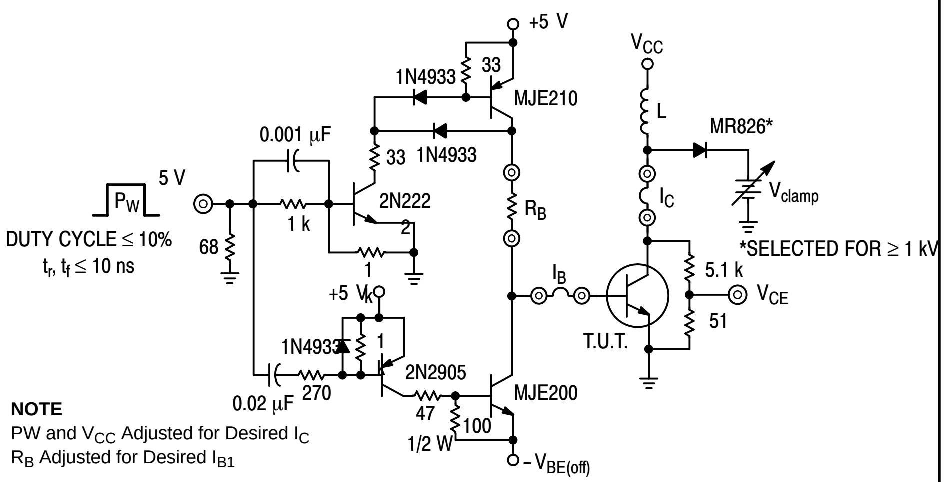
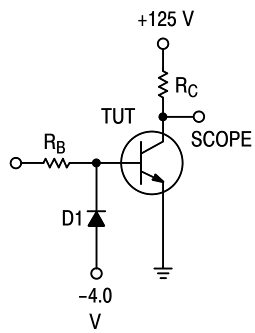


Figure 6. Capacitance

Table 1. Test Conditions for Dynamic Performance

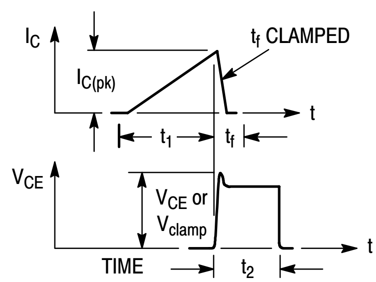
<table>
<tr><th></th><th>REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING</th><th>RESISTIVE SWITCHING</th></tr>
<tr><td>TEST CIRCUITS</td><td>


NOTE
PW and V_{CC} Adjusted for Desired I_C
R_B Adjusted for Desired I_{B1}
</td><td>


</td></tr>
<tr><td>CIRCUIT VALUES</td><td>Coil Data:
Ferroxcube Core #6656
Full Bobbin (~200 Turns) #20

GAP for 30 mH/2 A
L_{coil} = 50 mH

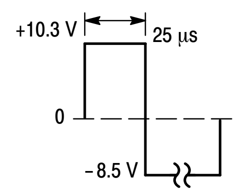
V_{CC} = 20 V
V_{clamp} = 300 Vdc</td><td>V_{CC} = 125 V
R_C = 125 Ω
D1 = 1N5820 or Equiv.
R_B = 47 Ω</td></tr>
<tr><td>TEST WAVEFORMS</td><td>
OUTPUT WAVEFORMS



t_1 Adjusted to Obtain I_C

$$t_1 \approx \frac{L_{coil}\,(I_{C_{pk}})}{V_{CC}}$$

$$t_2 \approx \frac{L_{coil}\,(I_{C_{pk}})}{V_{clamp}}$$

Test Equipment
Scope−Tektronics
475 or Equivalent
</td><td>


t_r, t_f < 10 ns
Duty Cycle = 1.0%
R_B and R_C adjusted for desired I_B and I_C
</td></tr>
</table>

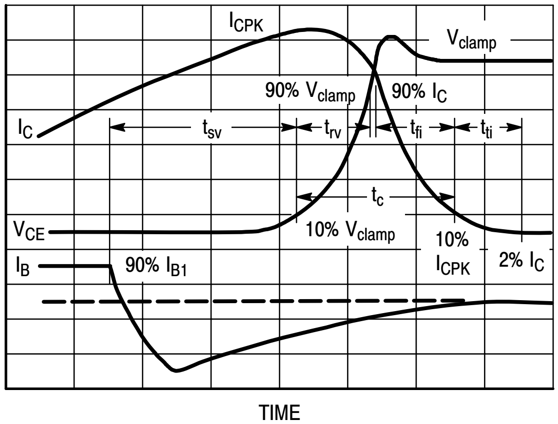


Figure 7. Inductive Switching Measurements

NOTE: All Data Recorded in the Inductive Switching Circuit in Table 1

Table 2. Typical Inductive Switching Performance

I_C AMP	T_C °C	t_{sv} μs	t_{rv} μs	t_{fi} μs	t_{ti} μs	t_c μs
0.5	25 100	1.3 1.6	0.23 0.26	0.30 0.30	0.35 0.40	0.30 0.36
1	25 100	1.5 1.7	0.10 0.13	0.14 0.26	0.05 0.06	0.16 0.29
1.5	25 100	1.8 3	0.07 0.08	0.10 0.22	0.05 0.08	0.16 0.28

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}

t_{rv} = Voltage Rise Time, 10−90% V_{clamp}

t_{fi} = Current Fall Time, 90−10% I_C

t_{ti} = Current Tail, 10−2% I_C

t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN−222:

$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

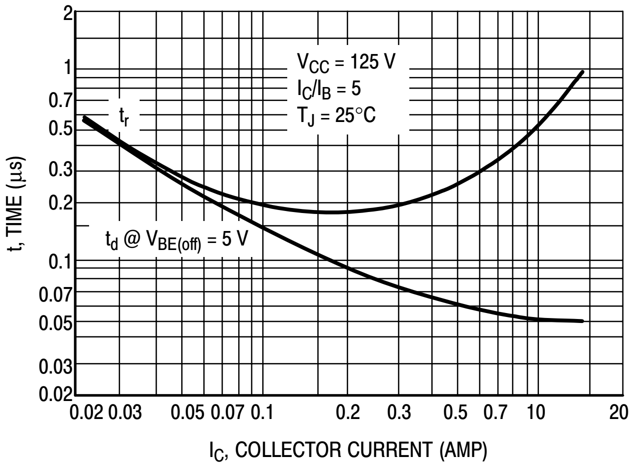


Figure 8. Turn−On Time

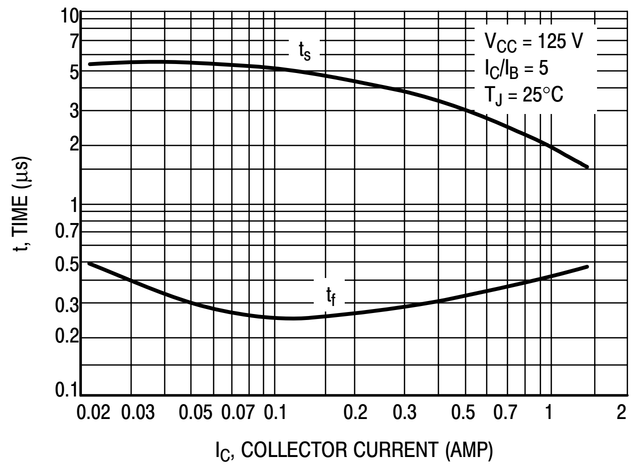


Figure 9. Turn−Off Time

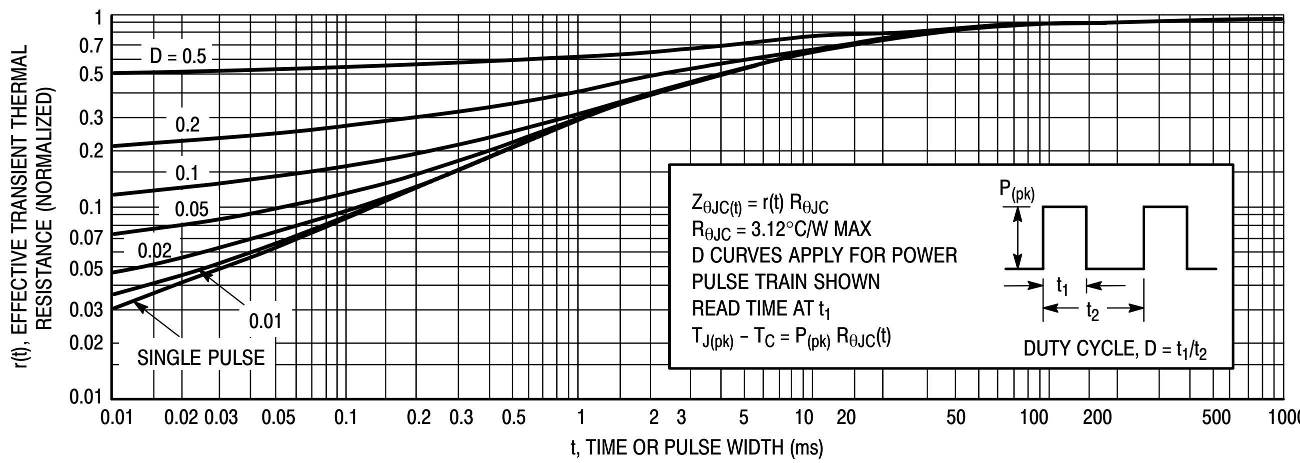


Figure 10. Thermal Response

The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

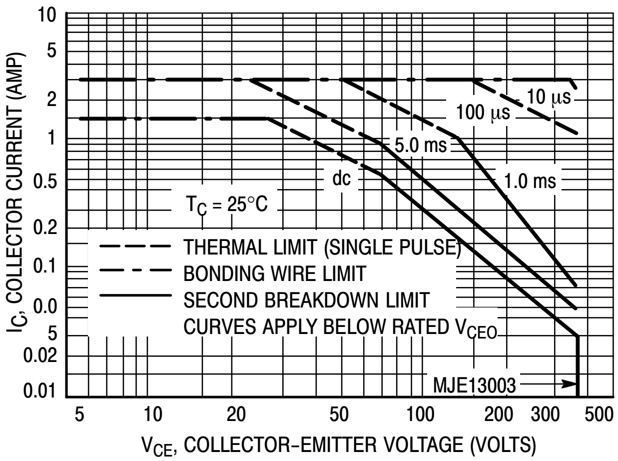


Figure 11. Active Region Safe Operating Area

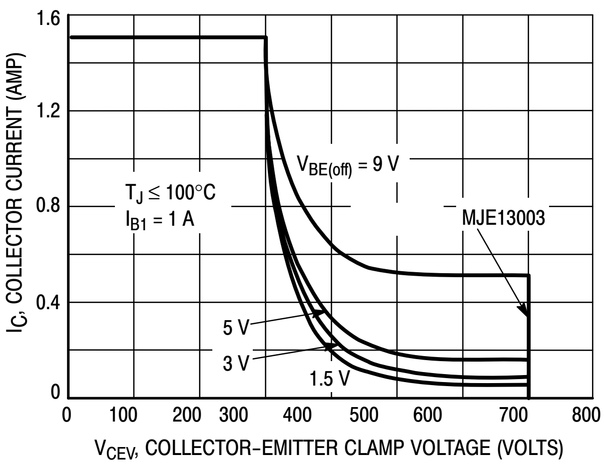


Figure 12. Reverse Bias Safe Operating Area

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn−off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage−current conditions during reverse biased turn−off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives RBSOA characteristics.

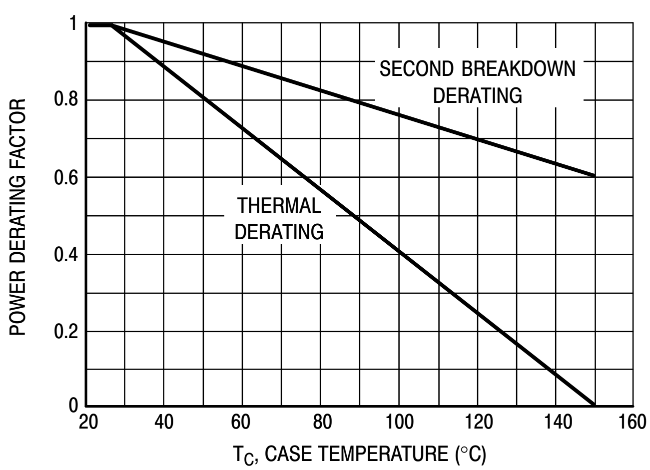
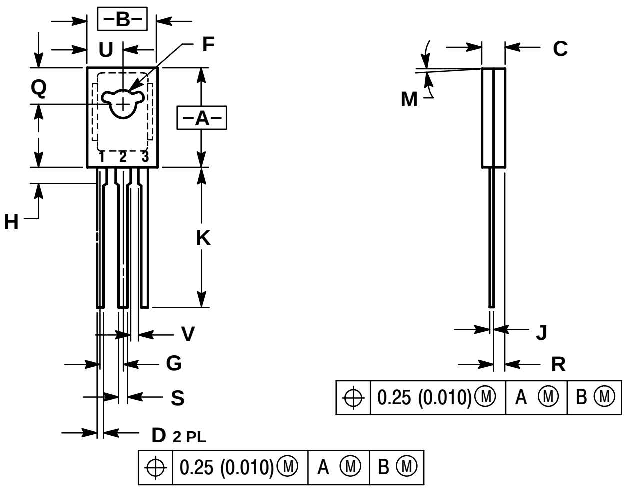


Figure 13. Forward Bias Power Derating

PACKAGE DIMENSIONS

TO−225
CASE 77−09
ISSUE Z



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 077−01 THRU −08 OBSOLETE, NEW STANDARD 077−09.

	INCHES		MILLIMETERS	
DIM	**MIN**	**MAX**	**MIN**	**MAX**
A	0.425	0.435	10.80	11.04
B	0.295	0.305	7.50	7.74
C	0.095	0.105	2.42	2.66
D	0.020	0.026	0.51	0.66
F	0.115	0.130	2.93	3.30
G	0.094 BSC		2.39 BSC	
H	0.050	0.095	1.27	2.41
J	0.015	0.025	0.39	0.63
K	0.575	0.655	14.61	16.63
M	5° TYP		5° TYP	
Q	0.148	0.158	3.76	4.01
R	0.045	0.065	1.15	1.65
S	0.025	0.035	0.64	0.88
U	0.145	0.155	3.69	3.93
V	0.040	---	1.02	---

STYLE 3:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

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